

1. A data processor which executes a program including a repeat block composed of plural instructions and processed repeatedly, said data processor comprising:

instruction execution inhibit means responsive to the detection of said
10 break of said repeat processing by said detecting means to inhibit the
execution of the remaining instructions in said repeat block.

3. The data processor according to claim 1, wherein said instruction
20 execution inhibit means is instruction processing sequence switching means
for switching said instruction processing sequence to the next instruction of
said repeat block at an instruction fetch stage upon detection of said break of
said repeat processing by said detecting means.

25 4. The data processor according to claim 1, wherein said instruction execution inhibit means is instruction processing sequence switching means for switching said instruction processing sequence to the next instruction of

5. The data processor according to claim 4, wherein said instruction processing sequence switching means is means for performing jump processing to the next instruction of said repeat block during execution of last instruction that is executed last in said repeat processing of said repeat block.

15 7. The data processor according to claim 1, wherein said detecting means is means for deciding whether said repeat processing breaks, based on an address of an instruction that is executed during said repeat processing of said repeat block.

8. The data processor according to claim 7, wherein said detecting means has count means for counting the number of repetitions of processing of said repeat block, and comparison means for comparing the address of the instruction to be currently processed in said repeat block with the address of the last instruction to be executed last in said repeat processing of said repeat block, and wherein upon being informed from said comparison means of the coincidence of address between said instruction to be currently processed and said last instruction when the count number of said count means has reached a

predetermined value, said detecting means decides that said repeat processing breaks.

9. The data processor according to claim 1, wherein said detecting
5 means is means for deciding whether said repeat processing breaks, based on the number of instructions to be executed during repeat processing of said repeat block.

10. The data processor according to claim 9, wherein said detecting
10 means has count means for counting the number of instructions executed during said repeat processing of said repeat block, and decides that said repeat processing breaks when the count number of said count means reaches a predetermined value.

11. The data processor according to claim 9, wherein said detecting
15 means has first count means for counting the number of repetitions of processing of said repeat block and second count means for counting the number of instructions executed during each repeat processing of said repeat block, and said detecting means decides that said repeat processing breaks
20 when the count number of said first count means reaches a first predetermined value and the count number of said second count means reaches a second predetermined value in the last repeat processing of said repeat block.